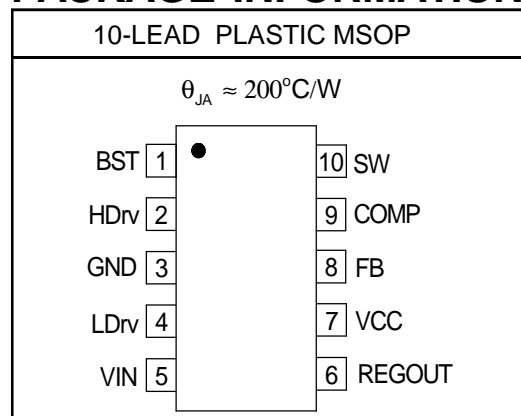


ABSOLUTE MAXIMUM RATINGS

VCC to GND & BST to SW voltage	-0.3V to 6.5V
VIN to GND	-0.3V to 30V
BST to GND Voltage	-0.3V to 35V
SW to GND	-2V to 35V
REGOUT to GND	0.2 to 16V
All other pins	-0.3V to 6.5V
Storage Temperature Range	-65°C to 150°C
Operating Junction Temperature Range	-40°C to 125°C
ESD Susceptibility	2kV

CAUTION: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc =5V, VIN=15V and T_A = 0 to 70°C. Typical values refer to T_A = 25°C.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V _{REF}			0.8		V
Ref Voltage line regulation				0.2		%
Supply Voltage(Vcc)						
V _{CC} Voltage Range	V _{CC}		4.75		5.25	V
Operating quiescent current	I _Q	EN=HIGH		3	5	mA
Vcc UVLO						
V _{CC} -Threshold	V _{CC_UVLO}	V _{CC} Rising		4.4		V
V _{CC} -Hysteresis	V _{CC_Hyst}	V _{CC} Falling		0.2		V
Supply Voltage(Vin)						
V _{in} Voltage Range	V _{in}		7		25	V
Input Voltage Current		Vin=24V		9	10	mA
Vin UVLO						
V _{in} -Threshold	V _{in_UVLO}	V _{CC} Rising		6		V

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
V _{in} -Hysteresis	V _{in-Hyst}	V _{CC} Falling		0.5		V
Oscillator (Rt)						
Frequency	F _s	NX2142		600		KHz
		NX2142A		1000		KHz
Frequency Over Vin			-5		5	%
Ramp-Amplitude Voltage	V _{RAMP}	Vin=20V		2		V
Ramp Offset				0.8		V
Ramp/Vin Gain				0.1		V/V
Max Duty Cycle				90		%
Min on time					150	nS
Error Amplifiers						
Transconductance				2500		umho
Input Bias Current	I _b				100	nA
Comp SD threshold				0.3		V
Soft Start						
Soft Start time	T _{ss}	NX2142		3.4		mS
		NX2142A		2		mS
High Side Driver(CL=3300pF)						
Output Impedance , Sourcing Current	R _{source} (Hdrv)	I=200mA		1		ohm
Output Impedance , Sinking Current	R _{sink} (Hdrv)	I=200mA		0.8		ohm
Rise Time	T _{Hdrv} (Rise)	10% to 90%		50		ns
Fall Time	T _{Hdrv} (Fall)	90% to 10%		50		ns
Deadband Time	T _{dead} (L to H)	Ldrv going Low to Hdrv going High, 10% to 10%		30		ns
Low Side Driver (CL=3300pF)						
Output Impedance, Sourcing Current	R _{source} (Ldrv)	I=200mA		1		ohm
Output Impedance, Sinking Current	R _{sink} (Ldrv)	I=200mA		0.5		ohm
Rise Time	T _{Ldrv} (Rise)	10% to 90%		50		ns
Fall Time	T _{Ldrv} (Fall)	90% to 10%		50		ns
Deadband Time	T _{dead} (H to L)	SW going Low to Ldrv going High, 10% to 10%		30		ns
Fixed OCP						
OCP voltage threshold				320		mV
FBUVLO						
Feedback UVLO threshold		percent of nominal	65	70	75	%
Over temperature						
Threshold				150		°C
Hysteresis				20		°C

PIN DESCRIPTIONS

PIN SYMBOL	PIN DESCRIPTION
VCC	This pin supplies the internal 5V bias circuit. A 1uF ceramic capacitor is placed as close as possible to this pin and ground pin.
BST	This pin supplies voltage to high side FET driver. A high freq minimum 0.1uF ceramic capacitor is placed as close as possible to and connected to this pin and SW pin.
GND	Power ground.
FB	This pin is the error amplifiers inverting input. This pin is connected via resistor divider to the output of the switching regulator to set the output DC voltage.
COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop.
SW	This pin is connected to source of high side FETs and provide return path for the high side driver.
HDRV	High side gate driver output.
LDRV	Low side gate driver output.
REGOUT	The output of the 5V regulator controller that drives a low current low cost external bipolar transistor or an external MOSFET to regulate the voltage at Vcc pin derived from bus voltage. This eliminates an otherwise external regulator needed in applications where 5V is not available. Regulator with 1uF ceramic output capacitor is stable.
VIN	Bus voltage input provides power supply to oscillator and VIN UVLO signal.

BLOCK DIAGRAM

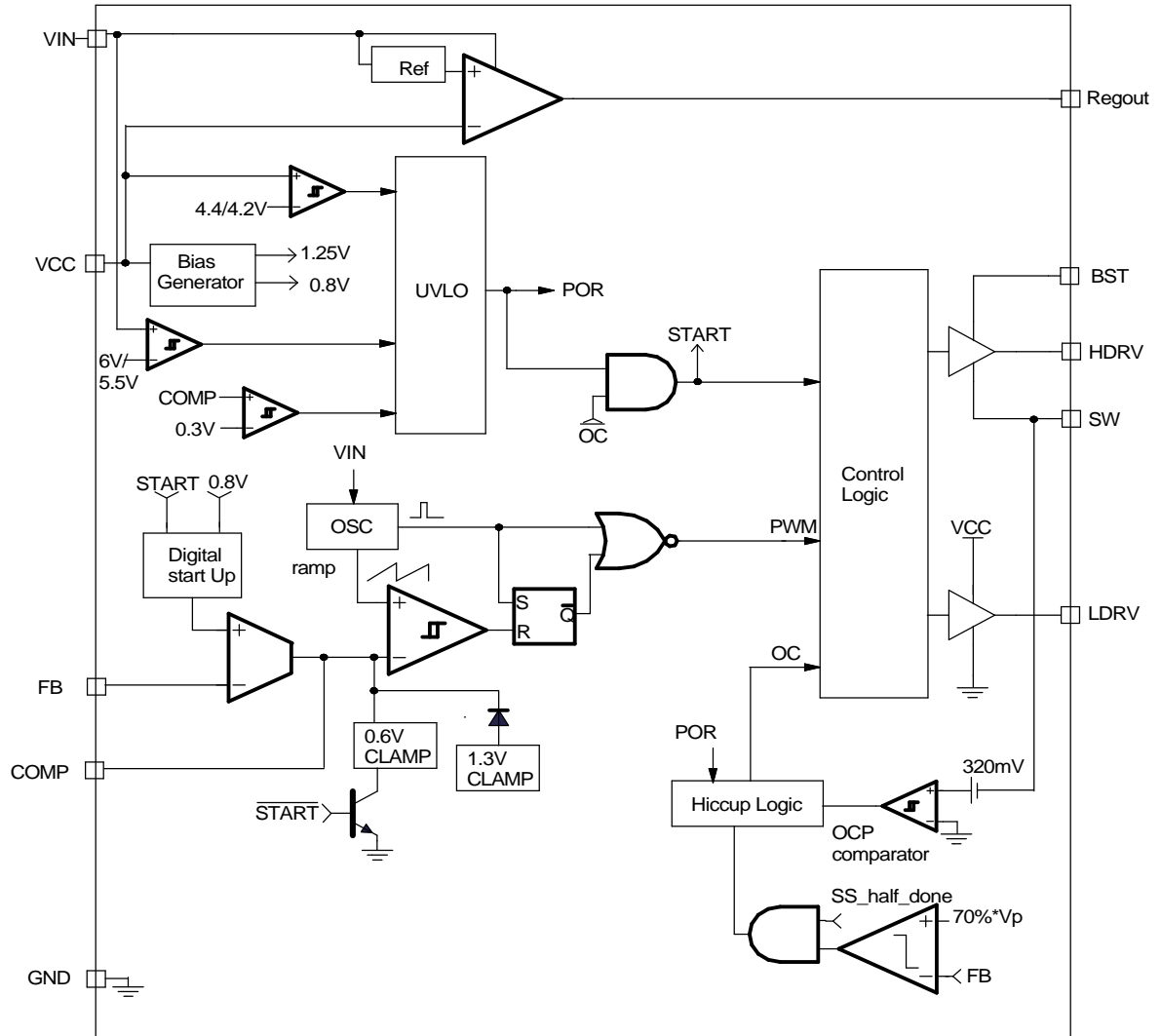


Figure 2 - Simplified block diagram of the NX2142

